IN THE CLAIMS:

Claims 1, 3, 6, 12, 16-21, 23, 25, 29, 31, 33, 36, 37, 39-44, and 46 have been amended herein. All of the pending claims 1 through 46 are presented below. This listing of claims will replace all prior versions and listings in the application. Please enter these claims as amended.

1. (Currently Amended) A semiconductor device, comprising:

a first functional die including at least a first bond pad;

at least a second functional die including at least a second bond pad and formed on a common semiconductor substrate with the first functional die; and

an adjacent die interconnection circuit operably coupling the at least a first bond pad of the first functional die with the at least a second bond pad of the at least a second functional die.

2. (Original) The semiconductor device, as recited in claim 1, wherein the adjacent die interconnection circuit includes at least one conductor segment having a first end electrically coupled to the at least a first bond pad and a second end electrically coupled to the at least a second bond pad.

3. (Currently Amended) The semiconductor device, as recited in claim 2, wherein the adjacent die interconnection circuit further includes a conductive bump electrically coupled to the at least one conductor segment configured for operatively coupling the at least one conductor segment of the semiconductor device with a substrate contact of a higher level packaging element.

4. (Original) The semiconductor device, as recited in claim 1, wherein the first functional die and the at least a second functional die are immediately adjacent.

5. (Original) The semiconductor device, as recited in claim 1, wherein the first functional die and the at least a second functional die are separated by at least one nonfunctional die.

6. (Currently Amended) The semiconductor device, as recited in claim 2, further comprising:

at least one nonfunctional die including at least one bond pad, the at least one nonfunctional die being formed on the common semiconductor substrate and located thereon between the first functional die and the at least a second functional die; and

wherein the at least one conductor segment extends between the at least a first bond pad and the at least one bond pad of the at least one nonfunctional die, the adjacent die interconnection circuit further including a second conductive segment extending between the at least one bond pad of the at least one nonfunctional die and the at least a second bond pad.

7. (Original) The semiconductor device, as recited in claim 6, further comprising a nonfunctional die bond pad isolation conductive segment including a first end electrically attached to the at least one conductor segment and the second conductive segment for coupling the at least a first bond pad of the first functional die with the at least a second bond pad of the at least a second functional die, the nonfunctional die bond pad isolation conductive segment further including a second end extending to the at least one nonfunctional die bond pad, the nonfunctional die bond pad isolation conductive segment being fabricated as an open circuit.

8. (Original) The semiconductor device, as recited in claim 6, wherein the at least one nonfunctional die further includes an isolation device coupled to the at least one bond pad of the at least one nonfunctional die for electrically isolating the at least one nonfunctional die from the adjacent die interconnection circuit.

9. (Original) A segment of a semiconductor wafer, comprising:

two or more functional dice each including at least one bond pad, the two or more functional dice being on a unitary semiconductor wafer segment; and

an adjacent die interconnection circuit for mutually operably coupling each at least one bond pad of the two or more functional dice to at least one other bond pad of the two or more functional dice.

10. (Original) The segment of a semiconductor wafer, as recited in claim 9, wherein the adjacent die interconnection circuit couples the two or more functional dice identified by testing of the semiconductor wafer to determine an operational status of each die on the semiconductor wafer.

11. (Original) The segment of semiconductor wafer, as recited in claim 9, wherein the adjacent die interconnection circuit includes a conductor segment for coupling between each of the two or more functional dice, the conductor segment including a first end electrically coupled to the at least one bond pad on one of the two or more functional dice and a second end electrically coupled to the at least one bond pad on another of the two or more functional dice.

12. (Currently Amended) The segment of semiconductor wafer, as recited in claim 9, further comprising:

at least one nonfunctional die including at least one bond pad, the nonfunctional die being formed on the ~~common semiconductor substrate~~ unitary semiconductor wafer segment and located thereon with the two or more functional dice; and

wherein the adjacent die interconnection circuit extends between the at least one bond pad of the at least one nonfunctional die to the at least one bond pad of the two or more functional dice.

13. (Original) The segment of semiconductor wafer, as recited in claim 9, wherein the two or more functional dice are immediately adjacent on the segment of semiconductor wafer.

14. (Original) The segment of semiconductor wafer, as recited in claim 9, wherein the two or more functional dice are separated by at least one nonfunctional die on the segment of semiconductor wafer.

15. (Original) A semiconductor wafer, comprising:

a plurality of dice each including a bond pad, the plurality of dice segregated according to functional dice and nonfunctional dice; and

an adjacent die interconnection circuit operably coupling a first bond pad of a first functional die with a second bond pad of a second functional die, the first functional die and the second functional die being operatively adjacent.

16. (Currently Amended) The semiconductor wafer, as recited in claim ~~11~~ 15, wherein the first functional die and the second functional die are immediately adjacent on the semiconductor wafer.

17. (Currently Amended) The semiconductor wafer, as recited in claim ~~11~~ 15, wherein the first functional die and the second functional die are separated by at least one nonfunctional die on the semiconductor wafer.

18. (Currently Amended) The semiconductor wafer, as recited in claim 15, wherein the adjacent die interconnection circuit includes at least one conductor segment having a first end electrically coupled to the ~~at least a~~ first bond pad and a second end electrically coupled to the ~~at least a~~ second bond pad for electrically coupling the ~~at least a~~ first bond pad with the ~~at least a~~ second bond pad.

19. (Currently Amended) The semiconductor wafer, as recited in claim 18, wherein the adjacent die interconnection circuit further includes a conductive bump electrically coupled to the at least one conductor segment configured for operatively coupling the at least one conductor segment of the semiconductor ~~device~~ wafer with a contact ~~of~~ of a higher level packaging.

20. (Currently Amended) The semiconductor wafer, as recited in claim 18, further comprising:

at least one nonfunctional die including at least one bond pad, the nonfunctional die being formed on ~~the~~ a common semiconductor substrate and located thereon between the first functional die and the ~~at least a~~ second functional die; and

wherein the at least one conductor segment extends between the ~~at least a~~ first bond pad and the at least one bond pad of the at least one nonfunctional die, the adjacent die interconnection circuit further including a second conductive segment extending between the at least one bond pad of the at least one nonfunctional die and the ~~at least a~~ second bond pad.

21. (Currently Amended) The semiconductor wafer, as recited in claim 20, further comprising a nonfunctional die bond pad isolation conductive segment including a first end electrically attached to the ~~at the~~ at least one conductor segment and the second conductive segment for coupling the ~~at least a~~ first bond pad of the first functional die with the ~~at least a~~ second bond pad of the ~~at least a~~ second functional die, the nonfunctional die bond pad isolation conductive segment further including a second end extending to the at least one bond pad of the nonfunctional die ~~bond pad~~, the nonfunctional die bond pad isolation conductive segment being fabricated as an open circuit.

22. (Original) The semiconductor wafer, as recited in claim 20, wherein the at least one nonfunctional die further includes an isolation device coupled to the at least one bond pad of

the at least one nonfunctional die for electrically isolating the at least one nonfunctional die from the adjacent die interconnection circuit.

23. (Currently Amended) A memory module, comprising:
a substrate including contacts extending to electrical connections to higher-level packaging; and
a semiconductor device, including:
a first functional die including at least a first bond pad;
at least a second functional die including at least a second bond pad; and
an adjacent die interconnection circuit operably coupling the at least a first bond pad of the first functional die with the at least a second bond pad of the at least a second functional die, the first functional die and the at least a second functional die being jointly fabricated on a single semiconductor substrate, the adjacent die ~~interconnect~~ interconnection circuit extending electrical connection to the contacts of the substrate.

24. (Original) The memory module, as recited in claim 23, wherein the adjacent die interconnection circuit includes at least one conductor segment having a first end electrically coupled to the at least a first bond pad and a second end electrically coupled to the at least a second bond pad.

25. (Currently Amended) The memory module, as recited in claim 24, wherein the adjacent die interconnection circuit further includes a conductive bump electrically coupled to the at least one conductor segment configured for operatively coupling the at least one conductor segment of the semiconductor device with the ~~substrate contact~~ contacts of the substrate.

26. (Original) The memory module, as recited in claim 23, wherein the first functional die and the at least a second functional die are immediately adjacent on the semiconductor device.

27. (Original) The memory module, as recited in claim 23, wherein the first functional die and the at least a second functional die are separated by at least one nonfunctional die on the semiconductor device.

28. (Original) The memory module, as recited in claim 24, further comprising:

at least one nonfunctional die including at least one bond pad, the nonfunctional die being formed on the common semiconductor substrate and located thereon between the first functional die and the at least a second functional die; and

wherein the at least one conductor segment extends between the at least a first bond pad and the at least one bond pad of the at least one nonfunctional die, the adjacent die interconnection circuit further including a second conductive segment extending between the at least one bond pad of the at least one nonfunctional die and the at least a second bond pad.

29. (Currently Amended) The memory module, as recited in claim 28, further comprising a nonfunctional die bond pad isolation conductive segment including a first end electrically attached to the ~~at the~~ at least one conductor segment and the second conductive segment for coupling the at least a first bond pad of the first functional die with the at least a second bond pad of the at least a second functional die, the nonfunctional die bond pad isolation conductive segment further including a second end extending to the at least one nonfunctional die bond pad, the nonfunctional die bond pad isolation conductive segment being fabricated as an open circuit.

30. (Original) The memory module, as recited in claim 28, wherein the at least one nonfunctional die further includes an isolation device coupled to the at least one bond pad of the at least one nonfunctional die for electrically isolating the at least one nonfunctional die from the adjacent die interconnection circuit.

31. (Currently Amended) An electronic system, comprising:

at least one processor device; and

at least one memory module for operably coupling with the at least one processor device, the at least one memory module including:

a substrate including contacts extending to electrical connections to higher-level packaging; and

a semiconductor device, including:

a first functional die including at least a first bond pad;

at least a second functional die including at least a second bond pad; and

an adjacent die interconnection circuit operably coupling the at least a first bond pad of the first functional die with the at least a second bond pad of the at least a second functional die, the first functional die and the at least a second functional die being jointly fabricated on a single semiconductor substrate, the adjacent die ~~interconnect~~ interconnection circuit extending electrical connection to the contacts of the substrate.

32. (Original) The electronic system, as recited in claim 31, wherein the adjacent die interconnection circuit includes at least one conductor segment having a first end electrically coupled to the at least a first bond pad and a second end electrically coupled to the at least a second bond pad.

33. (Currently Amended) The electronic system, as recited in claim 32, wherein the adjacent die interconnection circuit further includes a conductive bump electrically coupled to the at least one conductor segment configured for operatively coupling the at least one conductor segment of the semiconductor device with the ~~substrate contact~~ contacts of the substrate.

34. (Original) The electronic system, as recited in claim 31, wherein the first functional die and the at least a second functional die are immediately adjacent on the semiconductor device.

35. (Original) The electronic system, as recited in claim 31, wherein the first functional die and the at least a second functional die are separated by at least one nonfunctional die on the semiconductor device.

36. (Currently Amended) The electronic system, as recited in claim 32, further comprising:

at least one nonfunctional die including at least one bond pad, the nonfunctional die being formed on the ~~common~~ single semiconductor substrate and located thereon between the first functional die and the at least a second function die; and

wherein the at least one conductor segment extends between the at least a first bond pad and the at least one bond pad of the at least one nonfunctional die, the adjacent die interconnection circuit further including a second conductive segment extending between the at least one bond pad of the at least one nonfunctional die and the at least a second bond pad.

37. (Currently Amended) The electronic system, as recited in claim 36, further comprising a nonfunctional die bond pad isolation conductive segment including a first end electrically attached to the ~~at the~~ at least one conductor segment and the second conductive segment for coupling the at least a first bond pad of the first functional die with the at least a second bond pad of the at least a second functional die, the nonfunctional die bond pad isolation conductive segment further including a second end extending to the at least one nonfunctional die bond pad, the nonfunctional die bond pad isolation conductive segment being fabricated as an open circuit.

38. (Original) The electronic system, as recited in claim 36, wherein the at least one nonfunctional die further includes an isolation device coupled to the at least one bond pad of the at least one nonfunctional die for electrically isolating the at least one nonfunctional die from the adjacent die interconnection circuit.

39. (Currently Amended) A method of fabricating a semiconductor device, the method comprising:

forming a plurality of dice on a common semiconductor substrate, each of the plurality of dice including at least one bond pad;

identifying at least a first and second functional ~~dice~~ die from among at least a portion of the plurality of dice;

forming an adjacent die interconnection circuit between the at least one bond pad of the at least a first functional die and the at least one bond pad of the at least a second functional die; and

unitarily segmenting the at least ~~the~~ a first and second functional die from the common semiconductor ~~wafer~~ substrate.

40. (Currently Amended) The method, as recited in claim 39, wherein forming an adjacent die interconnection comprises forming at least one conductor segment having a first end electrically coupled to the at least one bond pad of the at least a first functional die and a second end electrically coupled to the at least one bond pad of the at least a second functional die.

41. (Currently Amended) The method, as recited in claim 40, wherein forming an adjacent die interconnection further comprises forming a conductive bump electrically coupled to the at least one conductor segment configured for operatively coupling the at least one conductor segment of the semiconductor device with a substrate contact of a higher-level assembly.

42. (Currently Amended) The method, as recited in claim 39, wherein identifying comprises identifying the at least a first and second functional ~~dice~~ die as immediately adjacent ones from among the at least a portion of the plurality of dice on the common semiconductor ~~wafer~~ substrate.

43. (Currently Amended) The method, as recited in claim 39, wherein identifying comprises identifying the at least a first and second functional ~~dice~~ die as separated by at least one nonfunctional ~~dice~~ die from among the at least a portion of the plurality of dice on the common semiconductor ~~wafer~~ substrate.

44. (Currently Amended) A method of functionally grouping a plurality of dice, comprising:

fabricating a plurality of dice on a common semiconductor substrate, at least a portion of the plurality of dice each including at least one bond pad;

identifying a plurality of functional and nonfunctional dice from among the at least a portion of the plurality of dice; and

electrically coupling the at least one bond pad of a first one of the plurality of functional dice with the at least one bond pad of at least a second one of the plurality of functional dice for ~~form~~ forming a functional group of dice on the common semiconductor substrate.

45. (Original) The method, as recited in claim 44, further comprising testing the functional group as a single assembly.

46. (Currently Amended) The method, as recited in claim 44, further comprising unitarily segmenting the functional group from the common semiconductor ~~wafer~~ substrate.

IN THE DRAWINGS:

The attached sheets of drawings include changes to FIGS. 3, 4A, and 4B. These sheets, which include FIGS. 3, 4A, and 4B, replace the original sheets including FIGS. 3, 4A, and 4B.